IESS 2007 - Final Program

(last update: 05/22/07)

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(a) Schedule

Time	Wednesday May 30, 2007	Thursday May 31, 2007	Friday June 1, 2007
7:30 AM - 8:30 AM		Breakfast	
8:30 AM - 9:45 AM	**Session 1** Opening Keynote 1	**Session 5** Opening Keynote 2	**Session 9** Opening Panel
9:45 AM - 10:00 AM		Coffee Break	
10:00 AM - 12:00 PM	**Session 2** Validation and Verification	**Session 6** Specification and Partitioning	**Session 10** Network on Chip
12:00 PM - 1:00 PM		Lunch Break	
1:00 PM - 3:10 PM	**Session 3** Automotive Applications	**Session 7** Tutorial 1 Design Methodologies	**Session 11** Tutorial 2 Medical Applications
3:10 PM - 3:30 PM		Coffee Break	
3:30 PM - 5:30 PM	**Session 4** Hardware Synthesis	**Session 8** Embedded Software	**Session 12** Distributed and Network Systems
5:30 PM - 6:00 PM			
6:00 PM - 10:00 PM	IFIP WG10.2 Meeting	Social Event	

Questions? Contact the Program Chair Rainer Dömer (doemer@uci.edu)

(b) Sessions

Wednesday, May 30, 2007

8:30 AM - 9:45 AM		**Session 1: Opening** Chair: Achim Rettberg (University of Paderborn, Germany)
8:30 AM - 8:45 AM	1.1	**Welcome to IESS 2007** *Achim Rettberg*, Mauro Zanella**, Franz Rammig*, Rainer Dömer***, Andreas Gerstlauer**** *University of Paderborn, Germany, **ZF Lemförder GmbH, Germany, ***University of California, Irvine
8:45 AM - 9:45 AM Keynote	1.2	**Where is System-Level Synthesis?** *Daniel D. Gajski* University of California, Irvine

10:00 AM - 12:00 PM		**Session 2: Validation and Verification** Chair: Samar Abdi (University of California, Irvine)
10:00 AM - 10:30 AM Best Paper Nominee	2.1	**Requirements and Concepts for Transaction Level Assertion Refinement** *Wolfgang Ecker, Volkan Esen, Thomas Steininger, Michael Velten* Infineon Technologies AG, Germany
10:30 AM - 11:00 AM	2.2	**Using a Runtime Measurement Device with Measurement-Based WCET Analysis** *Bernhard Rieder, Ingomar Wenzel, Klaus Steinhammer, Peter Puschner* Technical University of Wien, Austria
11:00 AM - 11:20 AM	2.3 (s)	**Implementing Real-Time Algorithms by using the AAA Prototyping Methodology** *Pierre Niang, Thierry Grandpierre, Mohamed Akil* ESIEE Paris, France
11:20 AM - 11:40 AM	2.4 (s)	**Run-Time efficient Feasibility Analysis of Uni-Processor Systems with Static Priorities** *Karsten Albers, Frank Bodmann, Frank Slomka* University of Ulm, Germany
11:40 AM - 12:00 PM	2.5 (c)	**Approach for Formal Verification of a Bit-serial Pipelined Architecture** *Henning Zabel, Achim Rettberg, Alexander Krupp* University of Paderborn, Germany

1:00 PM - 2:50 PM		**Session 3: Automotive Applications** Chair: Mauro Zanella (ZF Lemförder GmbH, Germany)
1:00 PM - 1:30 PM Best Paper Nominee	3.1	**Automotive System Optimization using Sensitivity Analysis** *Razvan Racu, Arne Hamann, Rolf Ernst* Technical University of Braunschweig, Germany
1:30 PM - 2:00 PM	3.2	**Towards a Dynamically Reconfigurable Automotive Control System Architecture** *R. Anthony*, A. Rettberg**, D. Chen***, I. Jahnich**, G. de Boer****, C. Ekelin***** (presenter: T. Qureshi***)* *U. of Greenwich, England, **U. of Paderborn, Germany, ***Royal Inst. of Tech., Sweden, ****Bosch, Germany, *****Volvo, Sweden
2:00 PM - 2:30 PM	3.3	**An OSEK/VDX-based Multi-JVM for Automotive Appliances** *Christian Wawersich, Michael Stilkerich, Wolfgang Schröder-Preikschat* University of Erlangen-Nuremberg, Germany
2:30 PM - 2:50 PM	3.4 (s)	**Towards Dynamic Load Balancing for Distributed Embedded Automotive Systems** *Isabell Jahnich, Achim Rettberg* University of Paderborn, Germany

3:30 PM - 5:30 PM		**Session 4: Hardware Synthesis** Chair: Luigi Carro (Federal University of Rio Grande do Sul, Brazil)
3:30 PM - 4:00 PM Best Paper Nominee	4.1	**Automatic Data Path Generation from C code for Custom Processors** *Jelena Trajkovic, Daniel Gajski* University of California, Irvine
4:00 PM - 4:30 PM	4.2	**Interconnect-aware Pipeline Synthesis for Array based Reconfigurable Architectures** *Shanghua Gao, Kenshu Seto, Satoshi Komatsu, Masahiro Fujita* University of Tokyo, Japan
4:30 PM - 4:50 PM	4.3 (s)	**An Interactive Design Environment for C-based High-Level Synthesis** *Dongwan Shin, Andreas Gerstlauer, Rainer Dömer, Daniel D. Gajski* University of California, Irvine
4:50 PM - 5:10 PM	4.4 (s)	**Integrated Coupling and Clock Frequency Assignment of Accelerators During Hardware/Software Partitioning** *Scott Sirowy, Frank Vahid* University of California, Riverside
5:10 PM - 5:30 PM	4.5 (c)	**Embedded Vertex Shader in FPGA** *Lars Middendorf, Felix Mühlbauer, Georg Umlauf, Christophe Bobda (presenter: Klaus Drechsler)* University of Kaiserslautern, Germany

Thursday, May 31, 2007

8:30 AM - 9:45 AM		**Session 5: Opening** Chair: Rainer Dömer (University of California, Irvine)
8:30 AM - 8:45 AM Best Paper Awards	5.1	**Best Paper Awards** *Rainer Dömer*, Mike Olivarez**, Flavio Wagner***, Hermann Kopetz***** *Univ. of California, Irvine, **Freescale Semiconductor, ***Fed. University of Rio Grande do Sul, ****Vienna University of Technology
8:45 AM - 9:45 AM Keynote	5.2	**Fine Granular Configurable RTOS for Ultra-low Resource Devices** *Franz Rammig* University of Paderborn, Germany

10:00 AM - 12:00 PM		**Session 6: Specification and Partitioning** Chair: Jianwen Zhu (University of Toronto, Canada)
10:00 AM - 10:30 AM	6.1	**A Hybrid Approach for System-Level Design Evaluation** *Alexander Viehl*, Markus Schwarz*, Oliver Bringmann*, Wolfgang Rosenstiel*** *FZI Forschungszentrum Informatik, Germany, **University of Tübingen, Germany
10:30 AM - 11:00 AM	6.2	**Automatic Parallelization of Sequential Specifications for Symmetric MPSoCs** *Fabrizio Ferrandi, Luca Fossati, Marco Lattuada, Gianluca Palermo, Donatella Sciuto, Antonino Tumeo* Politecnico di Milano, Italy
11:00 AM - 11:30 AM	6.3	**An Interactive Model Re-Coder for Efficient SoC Specification** *Pramod Chandraiah, Rainer Dömer* University of California, Irvine
11:30 AM - 12:00 PM	6.4	**Constrained and Unconstrained Hardware-Software Partitioning using Particle Swarm Optimization Technique** *M. B. Abdelhalim, A. E. Salama, S. E.-D. Habib* Cairo University, Egypt

1:00 PM - 3:10 PM		**Session 7: Design Methodologies** Chair: Andreas Gerstlauer (University of California, Irvine)
1:00 PM - 2:30 PM Tutorial	7.1	**Embedded SW Design Space Exploration and Automation using UML-Based Tools** *Flavio R. Wagner, Luigi Carro* Federal University of Rio Grande do Sul, Brazil
2:30 PM - 2:50 PM	7.2 (s)	**Using Aspect-Oriented Concepts in the Requirements Analysis of Distributed Real-Time Embedded Systems** *Edison P. Freitas*, Marco A. Wehrmeister**, Carlos E. Pereira*, Flavio R. Wagner*, Elias T. Silva Jr*, Fabiano C. Carvalho** *Universidade Federal do Rio Grande do Sul, Brazil, **University of Paderborn, Germany
2:50 PM - 3:10 PM	7.3 (c)	**Smart Speed TechnologyTM** *Mike Olivarez, Brian Beasley* Freescale Semiconductor, USA

3:30 PM - 5:30 PM		**Session 8: Embedded Software** Chair: Flavio R. Wagner (Federal University of Rio Grande do Sul, Brazil)
3:30 PM - 4:00 PM	8.1	**Power Optimization for Embedded System Idle Time in the Presence of Periodic Interrupt Services** *Gang Zeng, Hiroyuki Tomiyama, Hiroaki Takada* Nagoya University, Japan
4:00 PM - 4:30 PM	8.2	**Reducing the Code Size of Retimed Software Loops under Timing and Resource Constraints** *Noureddine Chabini*, Wayne Wolf*** *Royal Military College of Canada, **Princeton University
4:30 PM - 4:50 PM	8.3 (s)	**Identification and Removal of Program Slice Criteria for Code Size Reduction in Embedded Systems** *Mark Panahi, Trevor Harmon, Juan A. Colmenares, Shruti Gorappa, Raymond Klefstad* University of California, Irvine
4:50 PM - 5:10 PM	8.4 (s)	**Configurable Hybridkernel for Embedded Real-Time Systems** *Timo Kerstan, Simon Oberthür* University of Paderborn, Germany
5:10 PM - 5:30 PM	8.5 (c)	**Embedded Software Development in a System-Level Design Flow** *Gunar Schirner, Gautam Sachdeva, Andreas Gerstlauer, Rainer Dömer* University of California, Irvine

Friday, June 01, 2007

8:30 AM - 9:45 AM		**Session 9: Opening** Chair: Franz Rammig (University of Paderborn, Germany)
8:30 AM - 8:45 AM	9.1	**Announcement of IESS 2009** *Franz Rammig* University of Paderborn, Germany
8:45 AM - 9:45 AM Panel	9.2	**Modeling of Software-Hardware Complexes** *K.H. (Kane) Kim *, Wayne Wolf **, Nikil Dutt *, Hermann Kopetz ***, Franz J. Rammig ***** *University of California, Irvine, **Princeton University, ***Vienna University of Technology, ****University of Paderborn

10:00 AM - 12:00 PM		**Session 10: Network on Chip** Chair: Hiroyuki Tomiyama (Nagoya University, Japan)
10:00 AM - 10:30 AM	10.1	**Data Reuse Driven Memory and Network-On-Chip Co-Synthesis** *Ilya Issenin, Nikil Dutt* University of California, Irvine
10:30 AM - 11:00 AM	10.2	**Efficient and Extensible Transaction Level Modeling Based on an Object Oriented Model of Bus Transactions** *Rauf Salimi Khaligh, Martin Radetzki* University of Stuttgart, Germany
11:00 AM - 11:30 AM	10.3	**Hardware Implementation of the Time-Triggered Ethernet Controller** *Klaus Steinhammer, Astrit Ademaj* Vienna University of Technology, Austria
11:30 AM - 12:00 PM	10.4	**Error Containment in the Time-Triggered System-On-a-Chip Architecture** *R. Obermaisser, H. Kopetz, C. El Salloum, B. Huber* Vienna University of Technology, Austria

1:00 PM - 3:10 PM		**Session 11: Medical Applications** Chair: Mike Olivarez (Freescale Semiconductor, USA)
1:00 PM - 2:30 PM Tutorial	11.1	**Medical Embedded Systems** *Roozbeh Jafari *, Soheil Ghiasi**, Majid Sarrafzadeh**** *University of Texas at Dallas, **University of California, Davis, ***University of California, Los Angeles
2:30 PM - 2:50 PM	11.2 (s)	**Generic Architecture Designed for Biomedical Embedded Systems** *L. Sousa, M. Piedade, J. Germano, T. Almeida, P. Lopes, F. Cardoso, P. Freitas* Technical University of Lisbon, Portugal
2:50 PM - 3:10 PM	11.3 (c)	**A Small High Performance Microprocessor Core Sirius for Embedded Low Power Designs, Demonstrated in a Medical M** *Dirk Jansen, Nidal Fawaz, Daniel Bau, Marc Durrenberger* University of Applied Sciences, Offenburg, Germany

3:30 PM - 5:10 PM		**Session 12: Distributed and Network Systems** Chair: Carlos E. Pereira (Federal University of Rio Grande do Sul, Brazil)
3:30 PM - 4:00 PM	12.1	**Utilizing Reconfigurable Hardware to optimize Workflows in Networked Nodes** *Dominik Murr*, Felix Mühlbauer*, Falko Dressler**, Christophe Bobda* (presenter: Klaus Drechsler *)* *Kaiserslautern University of Technology, Germany, **University of Erlangen-Nuremberg, Germany
4:00 PM - 4:30 PM	12.2	**Dynamic Software Update of Resource-Constrained Distributed Embedded Systems** *Meik Felser, Rüdiger Kapitza, Jürgen Kleinöder, Wolfgang Schröder-Preikschat* University of Erlangen-Nuremberg, Germany
4:30 PM - 4:50 PM	12.3 (s)	**Configurable Medium Access Control for Wireless Sensor Networks** *Lucas F. Wanner, Augusto B. de Oliveira, Antônio A. Fröhlich* Federal University of Santa Catarina, Brazil
4:50 PM - 5:10 PM	12.4 (c)	**Integrating Wireless Sensor Networks and the Grid through POP-C++** *Augusto B. de Oliveira*, Lucas F. Wanner*, Pierre Kuonen**, Antônio A. Fröhlich ** *Federal University of Santa Catarina, Brazil, **University of Applied Sciences of Fribourg, Switzerland

Legend: (s) = Short paper
(c) = Case study
underlined = Speaker

Questions? Contact the Program Chair Rainer Dömer (doemer@uci.edu) (last update: 05/22/07)

(c) Program Highlights

Keynote Addresses

Wednesday, May 30, 2007
8:45 AM - 9:45 AM

Where is System-Level Synthesis?

Daniel D. Gajski
University of California, Irvine

Abstract:

With complexities of multi-core Systems-on-Chip (SOCs) rising almost daily, the design community has been searching for a new methodology that can handle given complexities with increased productivity and decreased time-to-market. The obvious solution that comes to mind is increasing levels of abstraction, or in other words, increasing the size of the basic building blocks. However, it is not clear what these basic blocks should be and what should be the strategy for composing a system design out of these basic blocks. To make things more difficult, the difference between software and hardware is becoming indistinguishable which, in turn, requires sizable change in the industrial and academic infrastructure.

In order to find the solution, we will look first at the system gap between SW and HW designs and derive requirements for the system design flow that includes software as well as hardware. In order to enable new tools for model generation, simulation, synthesis and verification, the design flow has to be supported by well defined abstraction levels, model semantics and transformations that correspond to design decisions made by designers. In order to satisfy those requirements we need some formalization of the design process. For this purpose, we will introduce the concept of model algebra that can serve as an enabler for the new strategy in system design and, consequently, system industry. Furthermore, we will demonstrate our approach on MP3 design and show increased simplicity and huge productivity gains for complex systems. We will explain the benefits and finish with a prediction and a roadmap toward the final goal of increasing productivity by several orders of magnitude while reducing expertise level needed for design of billion-transistor systems to the basic principles of design science only.

Thursday, May 31, 2007
8:45 AM - 9:45 AM

Fine Granular Configurable RTOS for Ultra-low Resource Devices

Franz Rammig
University of Paderborn, Germany

Abstract:

When designing a kernel for an operating system the developer has to choose between an microkernel or monolithic kernel approach. Bases for the decision is mostly the tradeoff between security and performance. Depending on application demands and on the available hardware a microkernel or a monolithic kernel approach or something between is desired. In this paper we present a hybrid kernel for embedded real-time systems which can be configured to the application demands in an easy way. To realize the hybrid kernel we present a technique to guarantee memory access in O(1) with virtual memory. With our approach the same codebase can be used for system services to be placed either in userspace or in kernelspace.

Panel Discussion

Friday, June 01, 2007
8:45 AM - 9:45 AM

Modeling of Software-Hardware Complexes

K.H. (Kane) Kim
University of California, Irvine

Abstract:

Various issues related to modeling of software-hardware complexes, including the following, will be addressed.
Are those currently available modeling approaches insufficient for use in systematic design and optimization of embedded software and hardware systems?
Are there potential synergies between software modeling and hardware modeling approaches?
What are the possibilities of and obstacles in combining some software modeling approaches and some hardware modeling approaches?
What are the kinds of things that software-modeling experts wish to learn from the work on hardware modeling?

Panelists:

Nikil Dutt, University of California, Irvine
Hermann Kopetz, Vienna University of Technology, Austria
Franz Rammig, University of Paderborn, Germany
Wayne Wolf, Princeton University
Kane Kim, University of California, Irvine

Tutorials

Thursday, May 31, 2007
1:00 PM - 2:30 PM

Embedded SW Design Space Exploration and Automation using UML-Based Tools
Flavio R. Wagner , *Luigi Carro*
Federal University of Rio Grande do Sul, Brazil

Abstract: This tutorial discusses design space exploration and software automation based on an UML front-end. First, we review software automation tools targeted at the embedded systems domain. Following, we present an approach for the estimation of memory, performance, and energy of a given application modeled from an initial UML specification. We proceed with an analysis of the possibilities of linking different modeling environments for software generation (Simulink and UML, for example). Finally, we show the possibilities of using other specification languages to obtain more abstraction and allow design space exploration together with software automation.

Friday, June 01, 2007
1:00 PM - 2:30 PM

Medical Embedded Systems
*Roozbeh Jafari *, Soheil Ghiasi**, Majid Sarrafzadeh****
*University of Texas at Dallas, **University of California, Davis, ***University of California, Los Angeles

Abstract: Light-weight embedded systems for medical monitoring are often referred to low-profile, small size, unobtrusive and potable processing elements with limited power resources. Such systems typically incorporate sensing, processing and communications and are often manufactured to be simple and cost-effective. Being low profile and wearable immediately implies the limitations in computational capabilities, memory (storage), speed and I/O interfaces. In this tutorial, we portray a brief description of low-power and light-weight embedded systems; present two pilot applications; and illustrate their corresponding design challenges. We specifically discuss the reconfiguration techniques.

Best Paper Awards

Thursday, May 31, 2007
8:30 AM - 8:45 AM

Best Paper Awards
*Rainer Dömer *, Mike Olivarez**, Flavio Wagner***, Hermann Kopetz*****
*Univ. of California, Irvine, **Freescale Semiconductor, ***Fed. University of Rio Grande do Sul, ****Vienna University of Technol

Committee:
Mike Olivarez (Freescale Semiconductor, USA)
Flavio Wagner (Federal University of Rio Grande do Sul, Brazil)
Herrmann Kopetz (Vienna University of Technology, Austria)

Nominees:

2.1 **Requirements and Concepts for Transaction Level Assertion Refinement**
Wolfgang Ecker, Volkan Esen, Thomas Steininger, Michael Velten
Infineon Technologies AG, Germany

3.1 **Automotive System Optimization using Sensitivity Analysis**
Razvan Racu, Arne Hamann, Rolf Ernst
Technical University of Braunschweig, Germany

4.1 **Automatic Data Path Generation from C code for Custom Processors**
Jelena Trajkovic, Daniel Gajski
University of California, Irvine

Selection:
The top three papers with the highest overall review score determined in the paper review process by the IESS Program Committee are nominated for the Best Paper Award. These papers are being presented at the first day of the conference.

The Best Paper Award Committee, composed of three members of the Program Committee, selects the order among the nominees and thus determines the winner of the Best Paper Award. The selection criteria are based on the quality of the presentation and the technical contribution of the paper.

The Best Paper Award will be announced in the opening session at the second day of the conference.

Social Event

Thursday, May 31, 2007 6:00 PM - 10:00 PM	**IESS Party** Las Brisas Restaurant 361 Cliff Drive Laguna Beach, CA 92651
Location:	The IESS party will be held on the outdoor patio of the Las Brisas restaurant providing seating and standing in a comfortable atmosphere. The restaurant is nestled in a scenic location on top of the cliffs of Laguna Beach, with walking access to the Pacific ocean and beaches. The menu will feature a buffet of items inspired by the cuisine of the Californian and Mexican Rivieras.
Admission:	All conference attendees and their guests are invited to attend in oder to mingle and exchange with their friends and colleagues in a relaxed environment. Admission to the event will be with ticket only. One ticket is provided as part of each full conference registration. Additional tickets to the event can be purchased for $80 each.
Transportation:	A shuttle bus will be available to provide transportation of conference attendees and their guests from the conference center and conference hotels to the Las Brisas restaurant and back. The shuttle bus will leave the conference center at approx. 6:00 PM and it will stop at the Atrium and Radisson hotels (appr 6:15-6:30 PM) for pickup before continuing on to the restaurant. On the return, the bus will pickup guests from Las Brisas at 10:00-10:15 PM for dropoff at the hotels or the conference center.

IFIP Meeting

Wednesday, May 30, 2007 6:00 PM - 8:00 PM	**IFIP WG10.2 Meeting** Balboa Room
(by invitation only)	The Working Group 10.2 (Embedded Systems, chaired by Wayne Wolf) of the International Federation for Information Processing (IFIP), who organizes the IESS Conference, will hold a meeting at the conference site. This meeting is for members and by invitation only.