Location

Beckman Conference Center
National Academies of
Sciences & Engineering
Irvine, California, USA

call for participation
May 30 - June 1, 2007
Irvine, California, USA
www.iess.org

IESS '07

INTERNATIONAL EMBEDDED SYSTEMS SYMPOSIUM

Wednesday, May 30, 2007

8:30 AM - 9:45 AM — 1. Opening — Chair: Achim Rettberg

8:30 AM - 8:45 AM — **Welcome to IESS 2007**
Achim Rettberg, Mauro Zanella, Franz Rammig, Rainer Doemer, Andreas Gerstlauer

8:45 AM - 9:45 AM — **Where is System-Level Synthesis?**
Keynote Daniel D. Gajski

10:00 AM - 12:00 PM — 2. Validation & Verification — Chair: TBD

10:00 AM - 10:30 AM — **2.1** — **Requirements and Concepts for Transaction Level Assertion Refinement**
Wolfgang Ecker, Volkan Esen, Thomas Steininger, Michael Velten

10:30 AM - 11:00 AM — **2.2** — **Using a Runtime Measurement Device with Measurement-Based WCET Analysis**
Bernhard Rieder, Ingomar Wenzel, Klaus Steinhammer, Peter Puschner

11:00 AM - 11:20 AM — **2.3 (s)** — **Implementing Real-Time Algorithms by using the AAA Prototyping Methodology**
Pierre Niang, Thierry Grandpierre, Mohamed Akil

11:20 AM - 11:40 AM — **2.4 (s)** — **Run-Time efficient Feasibility Analysis of Uni-Processor Systems with Static Priorities**
Karsten Albers, Frank Bodmann, Frank Slomka

11:40 AM - 12:00 PM — **2.5 (c)** — **Approach for a Formal Verification of a Bit-serial Pipelined Architecture**
Henning Zabel, Achim Rettberg, Alexander Krupp

1:00 PM - 2:50 PM — 3. Automotive Applications — Chair: Mauro Zanella

1:00 PM - 1:30 PM — **3.1** — **Automotive System Optimization using Sensitivity Analysis**
Razvan Racu, Arne Hamann, Rolf Ernst

1:30 PM - 2:00 PM — **3.2** — **Towards a Dynamically Reconfigurable Automotive Control System Architecture**
Richard Anthony, Achim Rettberg, Dejiu Chen, Isabell Jahnich, Gerrit de Boer, Cecilia Ekelin

2:00 PM - 2:30 PM — **3.3** — **An OSEK/VDX-based Multi-JVM for Automotive Appliances**
Christian Wawersich, Michael Stilkerich, Wolfgang Schröder-Preikschat

2:30 PM - 2:50 PM — **3.4 (s)** — **Towards Dynamic Load Balancing for Distributed Embedded Automotive Systems**
Isabell Jahnich, Achim Rettberg

3:30 PM - 5:30 PM — 4. Hardware Synthesis — Chair: TBD

3:30 PM - 4:00 PM — **4.1** — **Automatic Data Path Generation from C code for Custom Processors**
Jelena Trajkovic, Daniel Gajski

4:00 PM - 4:30 PM — **4.2** — **Interconnect-aware Pipeline Synthesis for Array based Reconfigurable Architectures**
Shanghua Gao, Kenshu Seto, Satoshi Komatsu, Masahiro Fujita

4:30 PM - 4:50 PM — **4.3 (s)** — **An Interactive Design Environment for C-based High-Level Synthesis**
Dongwan Shin, Andreas Gerstlauer, Rainer Dömer, Daniel D. Gajski

4:50 PM - 5:10 PM — **4.4 (s)** — **Integrated Coupling and Clock Frequency Assignment of Accelerators During Hardware/Software Partitioning**
Scott Sirowy, Frank Vahid

5:10 PM - 5:30 PM — **4.5 (c)** — **Embedded Vertex Shader in FPGA**
Lars Middendorf, Felix Mühlbauer, Georg Umlauf, Christophe Bobda

8:30 AM - 9:45 AM	**5. Opening**	Chair: Rainer Doemer	**Thursday, May 31, 2007**
8:30 AM - 8:45 AM	**Best Paper Awards**	Achim Rettberg, Mauro Zanella, Franz Rammig, Rainer Doemer, Andreas Gerstlauer	
8:45 AM - 9:45 AM	**Keynote**	**TBD** Franz Rammig	
10:00 AM - 12:00 PM	**6. Specification & Partitioning**	Chair: TBD	
10:00 AM - 10:30 AM	**6.1**	**A Hybrid Approach for System-Level Design Evaluation** Alexander Viehl, Markus Schwarz, Oliver Bringmann, Wolfgang Rosenstiel	
10:30 AM - 11:00 AM	**6.2**	**Automatic Parallelization of Sequential Specifications for Symmetric MPSoCs** Fabrizio Ferrandi, Luca Fossati, Marco Lattuada, Gianluca Palermo, Donatella Sciuto, Antonino Tumeo	
11:00 AM - 11:30 AM	**6.3**	**An Interactive Model Re-Coder for Efficient SoC Specification** Pramod Chandraiah, Rainer Dömer	
11:30 AM - 12:00 PM	**6.4**	**Constrained and Unconstrained Hardware-Software Partitioning using Particle Swarm Optimization Technique** M. B. Abdelhalim, A. E. Salama and S. E.-D. Habib	
1:00 PM - 3:10 PM	**7.Design Methodologies**	Chair: Andreas Gerstlauer	
1:00 PM - 2:30 PM	**7.1**	**Embedded SW Design Space Exploration and Automation using UML-Based Tools** Tutorial Flavio R. Wagner, Luigi Carro	
2:30 PM - 2:50 PM	**7.2 (s)**	**Using Aspect-Oriented Concepts in the Requirements Analysis of Distributed** Edison P. Freitas, Marco A. Wehrmeister, Carlos E. Pereira, Flavio R. Wagner, Elias T. Silva Jr, Fabiano C. Carvalho	
2:50 PM - 3:10 PM	**7.3 (c)**	**Smart Speed TechnologyTM** Mike Olivarez, Brian Beasley	
3:30 PM - 5:30 PM	**8. Embedded Software**	Chair: TBD	
3:30 PM - 4:00 PM	**8.1**	**Power Optimization for Embedded System Idle Time in the Presence of Periodic Interrupt Services** Gang Zeng, Hiroyuki Tomiyama, Hiroaki Takada	
4:00 PM - 4:30 PM	**8.2**	**Reducing the Code Size of Retimed Software Loops under Timing and Resource Constraints** Noureddine Chabini, Wayne Wolf	
4:30 PM - 4:50 PM	**8.3 (s)**	**Identification and Removal of Program Slice Criteria for Code Size Reduction in Embedded Systems Abstract Communication Modeling** Mark Panahi, Trevor Harmon, Juan A. Colmenares, Shruti Gorappa, Raymond Klefstad	
4:50 PM - 5:10 PM	**8.4 (s)**	**Configurable Hybridkernel for Embedded Real-Time Systems** Timo Kerstan, Simon Oberthür	
5:10 PM - 5:30 PM	**8.5 (c)**	**Embedded Software Development in a System-Level Design Flow** Gunar Schirner, Gautam Sachdeva, Andreas Gerstlauer, Rainer Dömer	
8:30 AM - 9:45 AM	**9. Opening**	Chair: TBD	**Friday, Juni 1, 2007**
8:30 AM - 8:45 AM		**Announcement of IESS 2009** Achim Rettberg, Mauro Zanella, Franz Rammig, Rainer Doemer, Andreas Gerstlauer	
8:45 AM - 9:45 AM	**Panel**	**Modeling of Software-Hardware Complexes** K.H. (Kane) Kim, Wayne Wolf, Nikil Dutt, Hermann Kopetz, Franz J. Rammig	
10:00 AM - 12:00 PM	**10. Network on Chip**	Chair: TBD	
10:00 AM - 10:30 AM	**10.1**	**Data Reuse Driven Memory and Network-On-Chip Co-Synthesis** Ilya Issenin, Nikil Dutt	
10:30 AM - 11:00 AM	**10.2**	**Efficient and Extensible Transaction Level Modeling Based on an Object Oriented Model of Bus Transactions** Rauf Salimi Khaligh, Martin Radetzki	
11:00 AM - 11:30 AM	**10.3**	**Hardware Implementation of the Time-Triggered Ethernet Controller** Klaus Steinhammer, Astrit Adem	
11:30 AM - 12:00 PM	**10.4**	**Error Containment in the Time-Triggered System-On-a-Chip Architecture** R. Obermaisser, H. Kopetz, C. El Salloum, B. Huber	
1:00 PM - 3:10 PM	**11. Medical Applications**	Chair: TBD	
1:00 PM - 2:30 PM	**11.1 Tutorial**	**Medical Embedded Systems** Roozbeh Jafari, Soheil Ghiasi, Majid Sarrafzadeh	
2:30 PM - 2:50 PM	**11.2 (s)**	**Generic Architecture Designed for Biomedical Embedded Systems** L. Sousa, M. Piedade, J. Germano, T. Almeida, P. Lopes, F. Cardoso, P. Freitas	
2:50 PM - 3:10 PM	**11.3 (c)**	**A Small High Performance Microprocessor Core Sirius for Embedded Low Power Designs, Demonstrated in a Medical Mass Application of an Electronic Pill (EPille®)** Dirk Jansen, Nidal Fawaz, Daniel Bau, Marc Durrenberger	
3:30 PM - 5:10 PM	**12. Distributed and Network Systems**	Chair: TBD	
3:30 PM - 4:00 PM	**12.1**	**Reconfigurable Hardware for optimizing Workflows in Networked Nodes** Dominik Murr, Felix Mühlbauer, Falko Dressler, Christophe Bobda	
4:00 PM - 4:30 PM	**12.2**	**Dynamic Software Update of Resource-Constrained Distributed Embedded Systems** Meik Felser, Rüdiger Kapitza, Jürgen Kleinöder, Wolfgang Schröder-Preikschat	
4:30 PM - 4:50 PM	**12.3 (s)**	**Configurable Medium Access Control for Wireless Sensor Networks** Lucas F. Wanner, Augusto B. de Oliveira, Antônio A. Fröhlich	
4:50 PM - 5:10 PM	**12.4 (c)**	**Integrating Wireless Sensor Networks and the Grid through POP-C++** Augusto B. de Oliveira, Lucas F. Wanner, Pierre Kuonen, Antônio A. Fröhlich	

Legend: (s) = Short paper (c) = Case study